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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/662,382	09/16/2003	Tomonori Kanai	4703-0101P	2172

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EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 08/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H'A

Office Action Summary	Application No.	Applicant(s)	
	10/662,382	KANAI ET AL.	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on June 9, 2005 has been received and entered in the case.

Claim Objections

2. Claim 1 is objected to because of the following informalities:

(A) In claim 1, line 12, "an internal electrode" should be --the internal electrodes--.

(B) In claim 1, lines 12 and 13, "and peripheral electrode" should be --and the peripheral electrodes--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1 – 4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

(A) In claim 1, line 11, "the same signal" lacks antecedent basis.

(B) Dependent claims 2 – 4 do not rectify the deficiency of claim 1 and therefore are similarly rejected.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1 and 3 – 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Seshan (U. S. Pat. No. 6,686,659).

Regarding claim 1, Seshan discloses in e.g., Fig. 11 a semiconductor device (500; column 8, line 64) comprising:

- peripheral electrodes (504; column 9, line 28 – 29) formed on a periphery of a semiconductor chip (500; column 8, line 64);
- internal electrodes (502; column 9, line 18) formed inside the peripheral electrodes on the semiconductor chip (see e.g., Fig. 11); and
- circuits (520; column 9, line 55) formed in the semiconductor chip,
- wherein the peripheral electrodes (504) are connected to the circuits by an internal line (i.e., 515; column 9, line 65), and the internal electrodes are connected to the circuits and the peripheral electrodes by the internal line (see e.g., Fig. 11 and column 10, lines 31 – 37), and
- wherein the same signal (any input or output signal from or to the circuit element 520; column 9, lines 55 – 58) is either an input and/or output either to or from both the internal electrodes and the peripheral electrodes (since the elements 502 and 504

are coupled together by an internal trace 515, the elements 502 and 504 receive same signal from the circuit element 520. see Fig. 11 and column 10, lines 31 – 37).

Regarding claims 3 and 7, Seshan discloses in e.g., Fig. 11 the internal electrodes comprising a power supply terminal (column 9, lines 16 – 18).

Regarding claims 4 and 8, Seshan discloses in e.g., Fig. 11, column 1, lines 39 – 43 and column 9, lines 55 – 58 the peripheral electrodes not connected to the internal electrodes being used as terminals for RF signals (since the circuit element 520 is radio frequency circuits, inherently, the input/output signals of the elements 504 are radio frequency signals).

Regarding claim 5, Seshan discloses in e.g., Fig. 11 a semiconductor device (510; column 9, line 51) comprising:

- peripheral electrodes (504; column 9, line 28 – 29) formed on a periphery of a semiconductor chip (500; column 8, line 64);
- internal electrodes (502; column 9, line 18) formed inside the peripheral electrodes on the semiconductor chip (see Fig. 11); and
- circuits (520; column 9, line 55) formed in the semiconductor chip,
- wherein the peripheral electrodes (504) are connected to the circuits by an internal line (i.e., 515; column 9, line 65), the internal electrodes (502) are connected to the circuits and the peripheral electrodes by the internal line (see Fig. 11 and column 10, lines 31 – 37), and the internal electrodes (502) are also connected to rewired lines (e.g., 603; column 10, line 3), the rewired lines formed above the internal electrodes with an insulating layer (600; column 9, lines 3 – 4) therebetween, and at ends of the rewired lines formed area array electrodes (i.e., 604 in Fig. 11).

Regarding claim 6, Seshan discloses in e.g., Fig. 11 a semiconductor device (510) comprising:

- peripheral electrodes (504) formed on a periphery of a semiconductor chip (500);
- internal electrodes (502) formed inside the peripheral electrodes on the semiconductor chip (see Fig. 11);
- area array electrodes (604, 608 and 610) connected to selected one of the peripheral electrodes and the internal electrodes and formed on the semiconductor chip; and
- circuits (520; column 9, line 55) formed in semiconductor chip,
- wherein the peripheral electrodes (504) are connected to the circuits by an internal line (i.e., 515; column 9, line 65), the internal electrodes (502) are connected to the circuits and the peripheral electrodes by the internal line (see Fig. 11 and column 10, lines 31 – 37), and the area array electrodes (604, 608 and 610) comprise first area array electrodes (604) connected to the internal electrodes (502) by rewired lines (603) and second area array electrodes (608 and 610) connected to the peripheral electrodes (504) by rewired lines (607 and 609).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Seshan in view of Arnold et al. (U. S. Pat. No. 4,521,449).

Seshan discloses the claimed invention except for the side of the internal electrodes being smaller than the peripheral electrodes. Arnold et al. teaches in Fig. 2 the side of internal electrodes (24; column 5, lines 14 and 15) being smaller than peripheral electrodes (42; column 3, line 50). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Seshan by using the small size of the internal electrodes of Arnold et al. into the internal electrodes of Seshan as taught by Arnold et al. The ordinary artisan would have been motivated to modify Seshan in the manner described above for at least the purpose of providing the density of vias to be less dense than the pads of the I/O connections to the device (column 3, lines 40 – 43).

9. Claims 1 – 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fang (U. S. Pat. No. 6,713,870).

Regarding claim 1, Fang discloses in e.g., Fig. 5 a semiconductor device (66; column 3, line 16) comprising:

- peripheral electrodes (511 and 512; column 2, lines 64 – 65) formed on a periphery of a semiconductor chip (66; column 3, line 16 and see Fig. 5);
- internal electrode (54; column 3, line 8) formed inside the peripheral electrodes on the semiconductor chip (see e.g., Fig. 5); and
- circuits (internal metal circuit layers on the element 611; column 3, lines 15 – 19) formed in the semiconductor chip,

- wherein the peripheral electrodes (511 an d512) are connected to the circuits by an internal line (anyone of the internal metal circuit layers on the element 611 and/or the element 55), and the internal electrode (54) is connected to the circuits and the peripheral electrodes (511) by the internal line (see e.g., Fig. 4).

While Fang discloses the internal electrode, Fang does not disclose a plurality of the internal electrodes. It would have been obvious to one having ordinary skill in the art at the time the invention was made to duplicate the internal electrode on the other part of the semiconductor chip, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. The ordinary artisan would have been motivated to modify Fang in the manner described above for at least the purpose of decreasing the complexity of the circuit layout under a redistribution consideration (column 2, lines 14 – 15). St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.

Regarding claim 2, Fang discloses in e.g., Fig. 5 the internal electrodes being smaller than the peripheral electrodes (see e.g., Fig. 5).

Regarding claim 3, Fang discloses in e.g., Fig. 5 the internal electrodes comprising a terminal (521). Furthermore, the term such as "power supply terminal", "ground terminal" or "clock terminal" is nothing more than a mere description of intended use of a terminal. Since the terminal (521) is capable of performing the intended use, the terminal (521) of Fang meets the claim.

Regarding claim 4, Fang discloses in e.g., Fig. 5 and column 1, lines 50 – 61 the peripheral electrodes not connected to the internal electrodes being used as terminals for high-frequency signals.

10. Claims 5 – 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fang (U. S. Pat. No. 6,713,870) in view of Galloway (U. S. Pat. No. 5,886,414).

Regarding claim 5, Fang discloses in e.g., Fig. 5 a semiconductor device comprising:

- peripheral electrodes (511 and 512; column 2, lines 64 – 65) formed on a periphery of a semiconductor chip (66; column 3, line 16 and see Fig. 5);
- internal electrode (54; column 3, line 8) formed inside the peripheral electrodes on the semiconductor chip (see Fig. 5); and
- circuits (internal metal circuit layers on the element 611; column 3, lines 15 – 19) formed in the semiconductor chip,
- wherein the peripheral electrodes (511 and 512) are connected to the circuits by an internal line (anyone of the internal metal circuit layers on the element 611 and/or the element 55), the internal electrode (54) is connected to the circuits and the peripheral electrodes by the internal line (see Fig. 5).

While Fang discloses the internal electrode, Fang does not disclose a plurality of the internal electrodes. It would have been obvious to one having ordinary skill in the art at the time the invention was made to duplicate the internal electrode on the other part of the semiconductor chip, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. The ordinary artisan would have been motivated to modify Fang in the manner described above for at least the purpose of decreasing the complexity of the circuit layout under a redistribution consideration (column 2, lines 14 – 15). St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.

Furthermore, while Fang discloses the internal electrode and area array electrodes, Fang does not disclose rewired lines. Galloway teaches in e.g., Fig. 1 internal electrode (16) being connected to rewired lines (12a), the rewired lines formed above the internal electrodes with an insulating layer (18'; column 2, lines 56 – 58) therebetween, and at ends of the rewired lines formed area array electrodes (24). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Fang by using the rewired lines of Galloway on the internal electrodes of Fang as taught by Galloway. The ordinary artisan would have been motivated to modify Fang in the manner described above for at least the purpose of increasing area for electrically contacting the die without changing the die design (column 3, lines 11 – 14).

Regarding claim 6, Fang discloses in e.g., Fig. 5 a semiconductor device comprising:

- peripheral electrodes (511 and 512) formed on a periphery of a semiconductor chip (66);
- internal electrode (54) formed inside the peripheral electrodes on the semiconductor chip (see Fig. 5);
- area array electrodes (521 and 522) connected to selected one of the peripheral electrodes and the internal electrodes and formed on the semiconductor chip; and
- circuits (internal metal circuit layers on the element 611; column 3, lines 15 – 19) formed in semiconductor chip,
- wherein the peripheral electrodes (511 and 512) are connected to the circuits by an internal line (anyone of the internal metal circuit layers on the element 611 and/or the element 55), the internal electrode (54) is connected to the circuits and the peripheral electrodes by the internal line (see Fig. 5), and the area array electrodes (521 and 522)

comprise first area array electrodes (521) connected to the internal electrodes (54) and second area array electrodes (522) connected to the peripheral electrodes (512) by rewired lines (532).

While Fang discloses the internal electrode, Fang does not disclose a plurality of the internal electrodes. It would have been obvious to one having ordinary skill in the art at the time the invention was made to duplicate the internal electrode on the other part of the semiconductor chip, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. The ordinary artisan would have been motivated to modify Fang in the manner described above for at least the purpose of decreasing the complexity of the circuit layout under a redistribution consideration (column 2, lines 14 – 15). St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.

Furthermore, while Fang discloses the internal electrode and area array electrodes, Fang does not disclose rewired lines. Galloway teaches in e.g., Fig. 1 first area array electrodes (24) connected to the internal electrodes (16) by rewired lines (12a). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Fang by using the rewired lines of Galloway on the internal electrodes of Fang as taught by Galloway. The ordinary artisan would have been motivated to modify Fang in the manner described above for at least the purpose of increasing area for electrically contacting the die without changing the die design (column 3, lines 11 – 14).

Regarding claim 7, Fang discloses in e.g., Fig. 5 the internal electrodes comprising a terminal (521). Furthermore, the term such as "power supply terminal", "ground terminal" or "clock terminal" is nothing more than a mere description of intended use of a terminal. Since the

terminal (521) is capable of performing the intended use, the terminal (521) of Fang meets the claim.

Regarding claim 8, Fang discloses in e.g., Fig. 5 and column 1, lines 50 – 61 the peripheral electrodes not connected to the internal electrodes being used as terminals for high-frequency signals.

Response to Arguments

11. Applicant's arguments filed on June 9, 2005 have been fully considered but they are not persuasive.

(A) Response to the Claim Rejections under 35 USC § 102(e)

On page 18, applicant argues that the newly amended claim 1 is not anticipated by Seshan. This argument is not persuasive because Seshan clearly discloses the newly added limitation in e.g., Fig. 11, column 9, lines 55 – 58 and column 10, lines 31 – 37 the same signal (any input or output signal from or to the circuit element 520; column 9, lines 55 – 58) being either an input and/or output either to or from both the internal electrodes and the peripheral electrodes (since the elements 502 and 504 are coupled together by an internal trace 515, the elements 502 and 504 receive same signal from the circuit element 520. see Fig. 11 and column 10, lines 31 – 37).

Since applicant has not responded or amended to the other independent claims 5 and 6 in the previous Office action, the rejection for the claims 5 – 8 is maintained.

For the above reasons, the rejection under 35 USC § 102(e) is maintained.

(B) Response to the Claim Rejections 1 – 8 under 35 USC § 103(a)

On page 19, applicant argues that Fang's metal wire 55 is not an internal line. This argument is not persuasive. Since applicant does not specifically claim that the internal line is formed inside of an insulating layer or a multi-layer, a reasonable interpretation of the term "internal line" includes the structure taught by Fang.

For the above reasons, the rejection is maintained.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chris C. Chu
Examiner
Art Unit 2815

c.c.
Monday, August 15, 2005

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER